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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Frequency divider

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Frequency divider

The invention relates to frequency divider.

Frequency dividers are widely used in modern communication devices for dividing a clock signal having a frequency and obtaining another signal having a lower frequency than the frequency of the clock signal. Usually, frequency dividers are implemented using flip-flops or latch circuits. Because clock signals are binary signals i.e. having a HIGH value level and a LOW level, frequency division factors, which are powers of 2 are relatively easier to be implemented.

In modern communication circuits, differential signals are often used and, as a direct consequence frequency dividers adapted to differential signals were necessary. US-A-6,166,571 describes a frequency divider circuit for producing output signals of half the frequency of an input clock signal, which comprises two identical circuit sections, each producing an output signal and its complement. The circuit sections are connected to each other so that the output signals of one circuit section serve as input signals to the other circuit section. Each circuit section contains a load transistor, which is controlled by one of the clock signal and the clock signal complement, and a switch transistor, which is controlled by the other of the clock signal and the clock signal complement. The circuit exhibits a reduced RC time constant for each circuit section and an increased output signal swing between the output signals and their respective complements. It is observed that the frequency divider comprises two identical sections that are both clocked by the clock signal. The higher the frequency the more dissipated power consummated.

There is therefore a need to have a differential frequency divider, which is operable at relatively high frequencies and consummating a relatively low power.

The invention is defined in the independent claim. The dependent claims define advantageous embodiments.

Because the second latch is no longer coupled to the clock signal, the total dissipated power is reduced.

The second latch may comprise a differential pair of transistors including a first pair of transistors comprising a first transistor coupled to second transistor, and a second

pair of transistor comprising third transistor coupled to a fourth transistor. Each transistor has a drain, a source and a gate. It should be pointed out here that the invention is not limited to MOS transistors implementation and in a bipolar implementation each transistor has a collector, an emitter and a base corresponding to the drains, source and gate, respectively. A drain of the first transistor and a drain of the third transistor are coupled to a source of the second transistor and to a source of the fourth transistor, respectively. Gates of the second transistor and fourth transistor receive a signal generated by the first latch. Gates of the first transistor and the third transistor are coupled to a control signal, for determining a low-pass characteristic of the second latch.

It is observed that the latch circuit behaves as a low-pass filter and amplifier. The control signals determine currents in the drains and sources of the first pair of transistors and the second pair of transistors, respectively, which, in turn, determines their amplifier and low-pass characteristics. Alternatively, if there is no need of control, the second transistor and the fourth transistor may be coupled directly to ground.

The control signal may be a DC signal, e.g. a voltage or a current, but it could be also a complementary clock signal to the clock signal supplied to the first latch.

When the control signal is a DC signal, the first latch behaves as a mixer circuit. The first latch receives an input signal having a frequency f_{in} and the second latch acts as a non-linear feedback loop. The first latch combines the input signal and the signal, which is fed back by the second latch, an output frequency of a signal generated by the second latch being a sub-harmonic of the input signal. The divider can make divisions by 2, 4, 6... etc. if there is a frequency multiplicative element inside the feedback loop. The non-linearity of the mixer behaves as a frequency multiplicative element and as the simulations verifies this new topology is able to make divisions by 2, 4 and 6 at the same power consumption as in the situation when the control signal is the complementary version of the clock signal applied to the first latch. It is further pointed out here that if one modifies the non-linearity of the feedback loop, divisions with factors as 3, 5, 7 are also possible. A worthwhile property of this divider is that it is able to reach higher frequencies without increasing te power consumption. This property enables the divider to reach to frequencies that is not possible by the standard D-FF based frequency dividers.

In the frequency divider, each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor, and between the drain of the fifth transistor and drain of the sixth transistor, respectively. The negative resistance is necessary for obtaining the latching property of the circuits and for having the necessary gain

in the latches. Usually, the negative resistance is obtained using a crossed coupled pair of transistors.

The above and other features and advantages of the invention will be apparent from the following description of the exemplary embodiments of the invention with reference to the accompanying drawings, in which:

Fig. 1 depicts a block schematic of a frequency divider, according to the invention,

Fig. 2a depicts an embodiment of a second latch circuit according to the invention,

Fig. 2b, depicts another embodiment of a second latch circuit according to the invention, and

Figs. 3a and 3b depict the principle of operation of the invention.

Fig. 1 depicts a block schematic of a frequency divider according to the invention. The divider comprises a first latch 10 and a second latch 20, the second latch 20 being crossed-coupled to the first latch. The first latch 10 comprises a clock input for receiving a clock signal, and the second latch 20 comprises a latch circuit configured as a low-pass filter. The first latch 10 comprises a first input I1 and a first complementary input I2 and a first output O1 and a first complementary output O2.

The second latch 20 comprises a second input I3 and a second complementary input I4 and a second output O3 and a second complementary out put O4. The outputs of the first latch 10 are coupled to the corresponding inputs of the second latch 20 i.e. O1 to I3 and O2 to I4. The outputs of the second latch 20 are coupled to the complementary inputs of the first latch 10 i.e. O3 to I2 and O4 to I1 i.e. the first latch 10 and the second latch are crossed-coupled. The first latch 10 receives a differential clock signal Ck, $\overline{Ck}$, and a pair of control signals C1 and C2 controls the second latch 20. At the second output O3 and at the second complementary output O4 there is obtained a signal having a frequency, which is fraction of a frequency of the clock signal.

Preferably, the second latch 20, as shown in Fig. 2a, comprises a differential pair of transistors M1, M3; M2, M4 including a first pair of transistors comprising a first transistor M1 coupled to second transistor M3. The second pair of transistor comprises third

transistor M2 coupled to a fourth transistor M4, each transistor having a drain, a source and a gate. It should be pointed out here that the invention is not limited to MOS transistors implementation and in a bipolar implementation each transistor has a collector, an emitter and a base corresponding to the drains, source and gate, respectively. A drain of the first transistor M1 and a drain of the third transistor M2 are coupled to a source of the second transistor M3 and to a source of the fourth transistor M4, respectively. Gates of the second transistor M3 and fourth transistor M4 receiving a signal generated by the first latch 10. Gates of the first transistor M1 and the third transistor M2 are coupled to a control signal C1, C2, for determining a low-pass characteristic of the second latch. In Fig. 2a, items having the same significance as in Fig. 1 are denoted by the same markings i.e. letters and figures.

It is observed that the latch circuit behaves as a low-pass filter and amplifier. The control signals C1 and C2 determine currents in the drains and sources of the first pair of transistors M1, M3 and the second pair of transistors M2, M4, respectively, which, in turn, determines their amplifier and low-pass characteristics. Alternatively, if there is no need of control, the second transistor and the fourth transistor may be coupled directly to ground as shown in Fig. 2b. In Fig. 2b, the second latch 20 comprises, a differential pair of transistors M1', M2' including a fifth transistor M1' and a sixth transistor M2'. A drain of the fifth transistor M1' and the drain of the sixth transistor M2' are coupled to supply voltage Vs via respective resistors R. A source of the fifth transistor M1' and a source of the sixth transistor M2' is coupled to a common potential e.g. ground. Gates of the fifth transistor M1' and sixth transistor M2' receive a signal generated by the first latch 10. In Fig. 2b, items having the same significance as is Fig. 2b are denoted by the same markings i.e. letters and figures. The control signals C1, C2 may be a DC signal, e.g. a voltage or a current.

Furthermore, C1 and C2 may be substantially equal to each other. The control signals may be a complementary clock signal to the clock signal supplied to the first latch.

When the control signal is a DC signal, the first latch behaves as a mixer circuit. The first latch 10 receives an input signal having a frequency f_{in} and the second latch acts as a non-linear feedback loop. The first latch 10 combines the input signal and the signal, which is fed back by the second latch 20, an output frequency of a signal generated by the second latch 20 being a sub-harmonic of the input signal. The divider can make divisions by 2, 4, 6... etc. if there is a frequency multiplicative element inside the feedback loop. It is further pointed out here that if one modifies the non-linearity of the feedback loop, divisions with factors as 3, 5, 7 are also possible.

The behavior of the frequency divider may be easier explained using the schematics shown in Figs. 3a and 3b. As seen in Fig. 3a the output signal f_{out} is fed back to the input of the mixer MIX. A low pass-filter filters out the higher frequency product coming from the mixer. If there is enough gain in the loop and the total phase shift is multiple of 2π than the following equality will be satisfied

$$f_{in} - f_{out} = f_{out} \rightarrow f_{in} = 2f_{out} \qquad (1)$$

If there is a frequency-multiplying element in the loop than it is even possible to make frequency divisions higher than two,

$$f_{in} - (N-1)f_{out} = f_{out} \rightarrow f_{in} = Nf_{out} \qquad (2)$$

The maximum input frequency of this division concept generally determined by the loop cut off frequency f_{max} , which is limited by both the mixer and the amplifier. Theoretically it is possible to make frequency divisions between the input frequencies $2f_{max}/3$ and $2f_{max}$. At input frequencies lower than $2f_{max}/3$ the product $f_{in}*f_{out}$ falls into the pass band of the low-pass filter. Therefore regenerative frequency divider has theoretically a minimum operating frequency. It may be shown that one of the factors determining the theoretical bandwidth ($2f_{max}/3$ - $2f_{max}$) is the order of the low-pass filter. Frequency division cannot be achieved if the low-pass filter is chosen as a first order filter. For third order or higher order filters the theoretically maximum possible bandwidth ($2f_{max}/3$ - $2f_{max}$) assumption becomes acceptable. When there is no input signal no output signal is obtained. The output signal is generated only when there is an input signal. The non-linearity of the mixer behaves as a frequency multiplicative element and as the simulations verifies this new topology is able to make divisions by 2, 4 and 6 at the same power consumption as in the situation when the control signal is the complementary version of the clock signal applied to the first latch. Without increasing the power consumption being able to reach to higher frequencies is a worth mentioning property of this divider. This property enables the divider to reach to frequencies that is not possible by the standard D-FF based frequency dividers.

In the frequency divider, each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor, and between the drain of the fifth transistor and drain of the sixth transistor, respectively. The negative resistance is

necessary for obtaining the latching property of the circuits and for having the necessary gain in the latches. Usually, the negative resistance is obtained using a crossed coupled pair of transistors, which are described as transistors pair M5, M6 in Figs. 2a and 2b.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed purpose processor. The invention resides in each new feature or combination of features.

CLAIMS:

1. A frequency divider comprising,
- a first latch (10) comprising a clock input for receiving a clock signal, and
- a second latch (20) comprising a latch circuit configured as a low-pass filter, the second latch (20) being crossed-coupled to the first latch.

2. A frequency divider as claimed in claim 1, wherein the second latch comprises
- a differential pair of transistors (M1, M3; M2, M4) including
- a first pair of transistors comprising a first transistor (M1) coupled to second transistor (M3),
- second pair of transistor comprising third transistor (M2) coupled to a fourth transistor (M4),
- each transistor having a drain, a source and a gate,
- a drain of the first transistor (M1) and a drain of the third transistor (M2) being coupled to a source of the second transistor (M3) and to a source of the fourth transistor (M4), respectively
- gates of the second transistor (M3) and fourth transistor (M4) receiving a signal generated by the first latch (10),
- gates of the first transistor (M1) and the third transistor (M2) being coupled to a control signal (C1, C2), for determining a low-pass characteristic of the second latch.

3. A frequency divider as claimed in claim 1, wherein the second latch comprises a differential pair of transistors (M1', M2') including
- a fifth transistor (M1') and a sixth transistor (M2'),
- each transistor having a drain, a source and a gate,
- a drain of the fifth transistor (M1') and the drain of the sixth transistor (M2') being coupled to supply voltage (Vs) via respective resistors,
- a source of the fifth transistor (M1') and a source of the sixth transistor (M2') being coupled to a common potential,

- gates of the fifth transistor (M1') and sixth transistor (M2') receiving a signal generated by the first latch (10).

4. A frequency divider as claimed in claim 2, wherein the control signal (C1, C2) is a DC signal.

5. A frequency divider as claimed in claim 2, wherein the control signal (C1, C2) is a complementary clock signal to the clock signal supplied to the first latch (10).

6. A frequency divider as claimed in claim 5, wherein the first latch (10) is substantially identical to the second latch (20).

7. A frequency divider as claimed in any of the preceding claims 2-6, wherein each latch comprises a negative resistance coupled between the drains of said second transistor (M3) and said fourth transistor (M4), and between the drain of the fifth transistor (M1') and drain of the sixth transistor (M6'), respectively.

ABSTRACT:

The invention refers to a frequency divider comprising, a first latch (10) and a second latch (20), the second latch (20) being crossed-coupled to the first latch. The first latch (10) comprises a clock input for receiving a clock signal, and the second latch (20) comprises a latch circuit configured as a low-pass filter.

Fig. 1

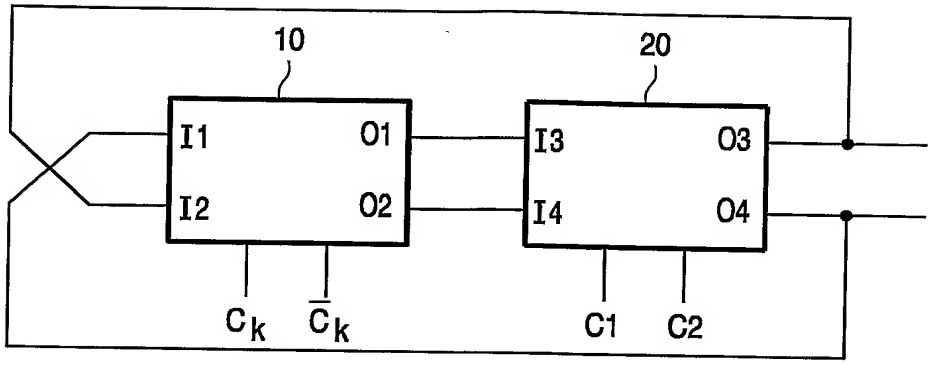

FIG. 1

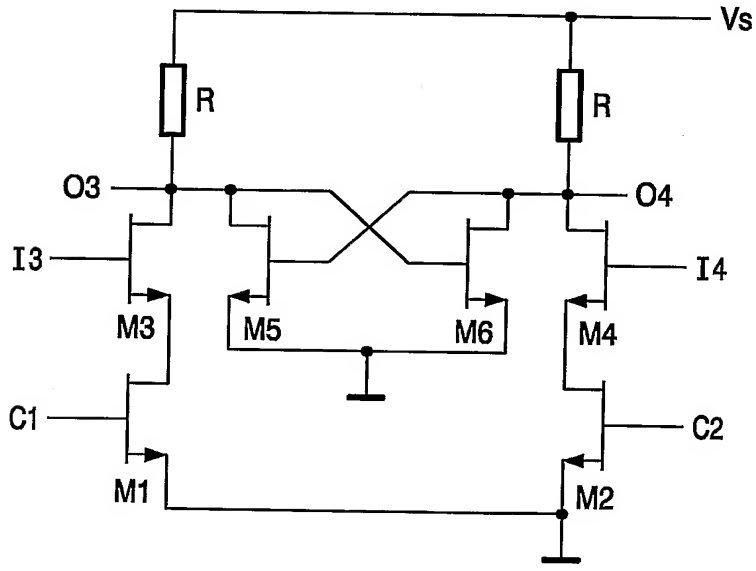

FIG. 2a

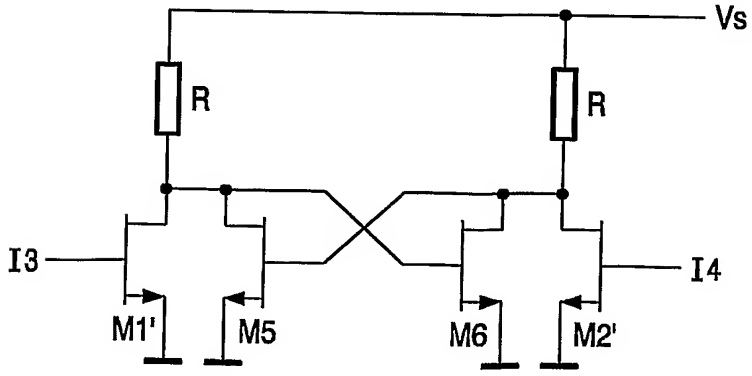

FIG. 2b

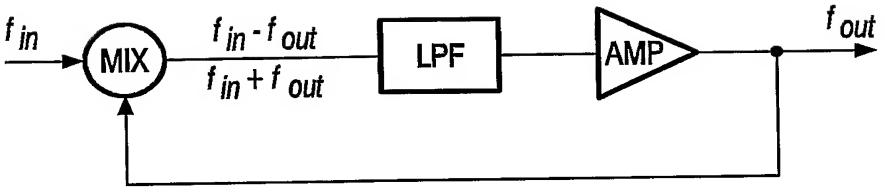
f in
MIX
f in - f out
f in + f out
LPF
AMP
f out

FIG. 3a

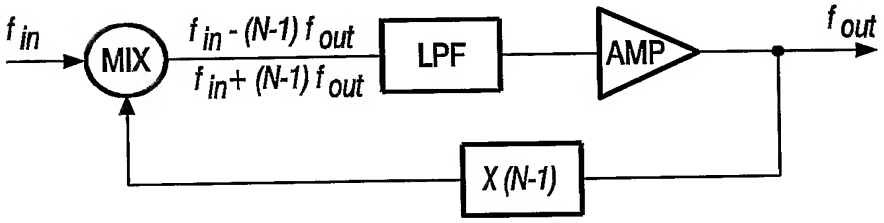
f in
MIX
f in - (N-1) f out
f in+ (N-1) f out
LPF
AMP
f out
X (N-1)

FIG. 3b